IN THE CLAIMS

1. (canceled)

2. (previously presented) An output buffer for a semiconductor device, comprising:
a driver stage comprising one or more drive transistors;
a pre-driver stage coupled to the driver stage; and
a feedback circuit to dynamically control output buffer impedance in response to a load condition;
wherein the feedback circuit comprises cascode-connected drive transistors.

3. (original) The output buffer of claim 2, wherein the driver and pre-driver stages comprise pull-up and pull-down sections.

4. (original) The output buffer of claim 3, further comprising one or more level shifter circuits.

5. (original) The output buffer of claim 4, wherein the output buffer is selectively configurable for operation at a plurality of supply voltages.

6. (previously presented) The output buffer of claim 2, further comprising a programmable interconnect to calibrate a rate of change in a signal level input to a pull-up or pull-down section of the output buffer.

7. (previously presented) The output buffer of claim 2, wherein the output buffer further comprises a programmable interconnect to selectively configure the output buffer for operation at a predetermined supply voltage range.

8. (original) The output buffer of claim 7, wherein the programmable interconnect is programmable during fabrication using at least one metal mask option.

9. (original) An output buffer for a flash memory device, comprising:
a pull-up driver coupled between a power supply node and an output node;
a pull-down driver coupled between a ground node and the output node;
a pull-up pre-driver coupled to the pull-up driver; and
a pull-down pre-driver coupled to the pull-down driver;
wherein the pull-up and pull-down drivers each comprise a plurality of cascode-connected drive transistors; and
wherein a gate of at least one of the cascode-connected drive transistors in each driver is coupled to the output node.

10. (original) The output buffer of claim 9, wherein the pull-up and pull-down pre-driver sections further comprise one or more level shifter circuits.

11. (original) The output buffer of claim 10, wherein the one or more level shifter circuits are selectively configurable for operation at a plurality of supply voltages.

12. (original) An output buffer for a semiconductor memory device, comprising:
a pull-down output driver stage, comprising:
a first NMOS pull-down transistor coupled between a ground node and an output pad, and
second and third NMOS pull-down transistors coupled in cascode between the ground node and the output pad, the second NMOS pull-down transistor comprising a gate coupled to a gate of the first NMOS pull-down transistor;
a pull-up output driver stage, comprising:
a first PMOS pull-up transistor coupled between a power supply node and the output pad, and
second and third PMOS pull-up transistors coupled in cascode between the power supply node and the output pad, the second PMOS pull-up transistor comprising a gate coupled to a gate of the first PMOS pull-up transistor

and the third PMOS pull-up transistor comprising a gate coupled to a gate of the third NMOS pull-down transistor;

a pull-up pre-driver stage coupled to the gate of the second PMOS pull-up transistor; and

a pull-down pre-driver stage coupled to the gate of the second NMOS pull-down transistor.

13. (original) The output buffer of claim 12, further comprising at least one programmable interconnect to selectively configure the output buffer to operate at a plurality of predetermined supply voltage ranges.

14. (original) The output buffer of claim 13, wherein the at least one programmable interconnect is programmable during fabrication using a metal mask option.

15. (original) The output buffer of claim 14, wherein the predetermined supply voltage range comprises 1.6 - 3.3V.

16. (original) The output buffer of claim 14, wherein the predetermined supply voltage range comprises an extended low-voltage range for a cellular telephone.

17. (original) The output buffer of claim 12, further comprising at least one programmable interconnect to adjust disoverlap of signal level inputs to pull-up and pull-down sections of the output buffer.

18. (canceled)

19. (original) A flash memory device, comprising:

an array of non-volatile memory cells; and

an output buffer coupled to the array, wherein the output buffer further comprises:

an output pad for providing a signal representative of a data value of a memory cell of the array;

a pull-down output driver stage, comprising:

a first NMOS pull-down transistor coupled between a ground node and the output pad, and

second and third NMOS pull-down transistors coupled in cascode between the ground node and the output pad, the second NMOS pull-down transistor comprising a gate coupled to a gate of the first NMOS pull-down transistor; and

a pull-up output driver stage, comprising:

a first PMOS pull-up transistor coupled between a power supply node and the output pad, and

second and third PMOS pull-up transistors coupled in cascode between the power supply node and the output pad, the second PMOS pull-up transistor comprising a gate coupled to a gate of the first PMOS pull-up transistor and the third PMOS pull-up transistor comprising a gate coupled to a gate of the third NMOS pull-down transistor.

20. (original) The flash memory device of claim 19, further comprising:

a pull-up pre-driver stage coupled to the gate of the second PMOS pull-up transistor for providing a first signal indicative of the data value; and

a pull-down pre-driver stage coupled to the gate of the second NMOS pull-down transistor for providing a second signal indicative of the data value.

21. (original) The flash memory device of claim 20, wherein each pre-driver stage has a level shifter comprising at least one programmable interconnect to selectively configure the level shifter to operate at a plurality of predetermined supply voltage ranges.

22. (original) The flash memory device of claim 21, wherein an input to each pre-driver stage is adapted to transition relatively quickly from a first logic level to a second logic level and relatively slowly from the second logic level to the first logic level.

23. (original) The flash memory device of claim 21, wherein one of the predetermined supply voltage ranges comprises 1.6 - 3.3V.

24. (original) A method for providing an impedance-adaptive output buffer for use in a flash memory device, comprising:
coupling a pull-up driver between a power supply node and an output node and
coupling a pull-down driver between a ground node and the output node;
coupling a pull-up pre-driver to the pull-up driver, and
coupling a pull-down pre-driver to the pull-down driver,
wherein the pull-up and pull-down drivers comprise cascode-connected output transistors.

25. (original) A method for providing an impedance-adaptive output buffer for use in a flash memory device, comprising:
providing feedback from an output node of the output buffer to a first cascode-connected transistor coupled between a power supply node and the output node; and
providing the feedback from the output node of the output buffer to a second cascode-connected transistor coupled between a ground node and the output node.

26. (canceled)

27. (currently amended) A method of dynamically adjusting the impedance of an output buffer for a semiconductor memory device, comprising:
reducing drive in a pull-up driver as a level of a signal on an output of the output buffer approaches a high logic level; and
reducing drive in a pull-down driver as a level of the signal on the output of the output buffer approaches a low logic level;
~~The method of claim 26~~ wherein reducing drive further comprises applying the signal on the output of the output buffer to a gate of a cascode-connected transistor of the driver.

28. (original) An output buffer, comprising:

a pull-up driver stage coupled to receive a first signal for coupling an output node of the output buffer to a supply potential node in response to the first signal having a first logic level and for presenting a high impedance to the output node in response to the first signal having a second logic level; and

a pull-down driver stage coupled to receive a second signal for coupling the output node to a ground potential node in response to the second signal having the second logic level and for presenting a high impedance to the output node in response to the second signal having a first logic level;

wherein the pull-up driver stage comprises at least two cascode-connected transistors coupled between the supply potential node and the output node with at least one of its cascode-connected transistors coupled to receive the first signal on its gate and at least one of its cascode-connected transistors having its gate coupled to the output node; and

wherein the pull-down driver stage comprises at least two cascode-connected transistors coupled between the ground potential node and the output node with at least one of its cascode-connected transistors coupled to receive the second signal on its gate and at least one of its cascode-connected transistors having its gate coupled to the output node.

29. (original) The output buffer of claim 28, wherein the pull-up driver stage further comprises:

at least one transistor coupled in parallel with its cascode-connected transistors between the supply potential node and the output node and having its gate coupled to receive the first signal.

30. (original) The output buffer of claim 28, wherein the pull-down driver stage further comprises:

at least one transistor coupled in parallel with its cascode-connected transistors between the ground potential node and the output node and having its gate coupled to receive the second signal.

31. (original) An electronic system, comprising:

an array of non-volatile memory cells;

a processor; and

an input/output (I/O) circuit for providing bi-directional communications between the processor and the array of non-volatile memory cells;

wherein the I/O circuit includes an output buffer having an output node, the output buffer comprising:

a pull-up pre-driver section coupled to receive a first signal indicative of a data value of a memory cell of the array;

a pull-down pre-driver section coupled to receive a second signal indicative of the data value of the memory cell of the array, wherein the first signal and the second signal are generally of the same logic level;

a pull-up driver stage coupled to receive an output signal from the pull-up pre-driver section for coupling the output node to a supply potential node in response to the first signal having a first logic level and for presenting a high impedance to the output node in response to the first signal having a second logic level; and

a pull-down driver stage coupled to receive an output signal from the pull-down pre-driver section for coupling the output node to a ground potential node in response to the second signal having the second logic level and for presenting a high impedance to the output node in response to the second signal having a first logic level;

wherein each driver stage comprises feedback circuitry to dynamically control an impedance of the output buffer in response to a load condition between the output buffer and the processor.

32. (original) The electronic system of claim 31, wherein the feedback circuitry for the pull-up driver stage comprises a cascode-connected transistor coupled between the supply potential node and the output node and wherein a gate of the cascode-connected transistor is coupled to the output node.

33. (original) The electronic system of claim 31, wherein the feedback circuitry for the pull-down driver stage comprises a cascode-connected transistor coupled between the ground potential node and the output node and wherein a gate of the cascode-connected transistor is coupled to the output node.

34. (original) The electronic system of claim 31, further comprising:

wherein the pull-up driver stage comprises at least two cascode-connected transistors coupled between the supply potential node and the output node with at least one of its cascode-connected transistors coupled to receive the output signal from the pull-up pre-driver stage on its gate and at least one of its cascode-connected transistors having its gate coupled to the output node; and

wherein the pull-down driver stage comprises at least two cascode-connected transistors coupled between the ground potential node and the output node with at least one of its cascode-connected transistors coupled to receive the output signal from the pull-down pre-driver stage on its gate and at least one of its cascode-connected transistors having its gate coupled to the output node.

35. (original) A method of fabricating an output buffer for a semiconductor device, comprising:

selecting between operation at a first supply potential or a second supply potential, wherein the second supply potential is higher than the first supply potential;

fabricating transistors of driver and pre-driver sections of the output buffer to have a first thickness for the first supply potential or a second thickness for the second supply potential, wherein the second thickness is higher than the first thickness;

fabricating the transistors to have a first doping level for the first supply potential or a second doping level for the second supply potential, wherein the second doping level is lower than the first doping level;

fabricating the transistors to have a first gate length for the first supply potential or a second gate length for the second supply potential, wherein the second gate length is longer than the first gate length and wherein a space to accommodate the second gate length is provided whether the first gate length or the second gate length is chosen; and

fabricating a pull-down stage of a level shifter of the output buffer to have a first size for the first supply potential and a second size for the second supply potential, wherein the first size is smaller than the second size, and wherein the size of the pull-down stage is determined by programming of one or more programmable interconnects to selectively engage or disengage circuit elements of the level shifter.

36. (original) The method of claim 35, wherein programming of the one or more programmable interconnects occurs during fabrication.

37. (original) The method of claim 36, wherein programming of the one or more programmable interconnects comprises selecting metal mask options.

38. (original) The method of claim 35, wherein programming of the one or more programmable interconnects occurs post-production using programmable interconnects selected from the group consisting of jumpers, fusible links, electrically programmable links and optically programmable links.

39. (original) The method of claim 35, further comprising:
fabricating a pull-up stage of the level shifter of the output buffer to have a first size for the first supply potential and a second size for the second supply potential, wherein the first size is smaller than the second size, and wherein the size of the pull-up stage is determined by programming of one or more programmable interconnects to selectively engage or disengage circuit elements of the level shifter.